

What is Claimed is:

1. A method for dynamically writing to an internal
5 register space of a chip using a test access port
("TAP") controller without interfering with normal
operation of the chip, comprising:
loading write instructions and address of the
internal register space where data is to be
10 written; and
gaining access through arbitration to the internal
register space.
2. The method of Claim 1, wherein data that is to be
written is loaded into a register in the TAP
15 controller before being written in the internal
register space.
3. The method of Claim 1, wherein the write
instructions are loaded into an instruction
register of the TAP controller.
- 20 4. A method for dynamically reading from an internal
register space of a chip using a test access port
("TAP") controller without interfering with normal
operation of the chip, comprising:
loading a read command in an instruction register;
25 loading an address of the internal register space
from where data is to be read, to a data register;

gaining access to the internal register space; and
transferring information to a register in the TAP
controller.

5. The method of Claim 4, wherein access to the
5 internal register space is gained using an
arbitration module.
6. The method of Claim 4, wherein the instruction
register is located in the TAP controller.
7. A system of accessing an internal register space of
10 a chip using a test access port ("TAP") controller
without interfering with normal operation of the
chip, comprising:
an instruction register in the TAP controller to
which read and/or write instructions are written;
15 and
an arbitration module that receives an input from
the TAP controller when the TAP controller needs to
access the internal register space.
8. The system of Claim 7, wherein write instructions
20 are loaded in the instruction register and address
of the internal register space where data is to be
written is loaded into a data register.
9. The system of Claim 7, wherein an address of the
internal register space from where data is to be
25 read is loaded to the data register.

10. The system of Claim 7, wherein after the TAP controller reads data from the internal register space it is stored in the data register.
11. The system of Claim 10, wherein data that is to be
5 written into the internal register space is first written to the data register.
12. A test access port ("TAP") controller for dynamically accessing an internal register space in a chip without interfering with normal operation of
10 the chip, comprising:
an instruction register in the TAP controller to which read and/or write instructions are written;
and
a data register where data is stored after the TAP
15 controller reads it from the internal register space, and/or data that is to be written into the internal register is first written to the data register.
13. The TAP controller of Claim 12, wherein before
20 accessing the internal register space, the TAP controller requests access to an arbitration module.